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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,247	07/21/2003	Gurkanwal Sahota	990307C1	7330

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QUALCOMM INCORPORATED
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EXAMINER	
VUONG, QUOCHIEN B	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,247	SAHOTA ET AL	
	Examiner	Art Unit	
	Quochien B. Vuong	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/21/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-32 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 31-51 and 63-73 of U.S. Patent No. 6,615,027. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claim 1 of the present application, claim 31 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including a device comprising: an interface circuit formed on a first integrated circuit (IC) for generating a differential current signal responsive to a reference signal and to a digital data input; and a circuit

element formed external of the first IC for generating an output signal on the basis of the differential current signal.

Regarding claim 2 of the present application, claim 32 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the device is a transmitter.

Regarding claim 3 of the present application, claim 34 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the device is a CDMA telephone.

Regarding claim 4/(1,2, or 3) of the present application, claim 35 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the reference signal is generated by a reference circuit on at least one of a second IC or coupled to the second IC.

Regarding claim 5/(1,2, or 3) of the present application, claim 36 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including a reference circuit for generating the reference signal.

Regarding claim 6/(1,2, or 3) of the present application, claim 37 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including at least one capacitor coupled between the differential current signal.

Regarding claim 7/(1,2, or 3) of the present application, claim 38 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.

Regarding claim 8 of the present application, claim 33 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the transmitter is a quadrature transmitter.

Regarding claim 9/(1,2, or 3) of the present application, claim 39 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the reference signal is a voltage reference signal.

Regarding claim 10/(1,2, or 3) of the present application, claim 40 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the voltage reference signal is generated on the basis of a bandgap reference voltage.

Regarding claim 11/(1,2, or 3) of the present application, claim 41 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the reference signal is a current generated from a reference voltage and a resistor.

Regarding claim 12 of the present application, claim 42 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the output signal is a voltage signal and the resistor is external to the first and second ICs.

Regarding claim 13 of the present application, claim 43 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the output signal is a current signal and the resistor is implemented on the second IC.

Regarding claim 14/(1,2, or 3) of the present application, claim 44 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the interface circuit includes a current mirror for generating at least two mirror paths using the

reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.

Regarding claim 15/(1,2, or 3) of the present application, claim 45 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the digital data input is at least a four bit digital data input.

Regarding claim 16/(1,2, or 3) of the present application, claim 46 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the digital data input is an oversampled digital data signal.

Regarding claim 17/(1,2, or 3) of the present application, claim 47 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.

Regarding claim 18/(1,2, or 3) of the present application, claim 48 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the circuit element is a modulator.

Regarding claim 19 of the present application, claim 49 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.

Regarding claim 20 of the present application, claim 50 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein each current source in the modulator provides a bias current that is related to the reference signal.

Regarding claim 21 of the present application, claim 51 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the modulator performs direct up conversion.

Regarding claim 22 of the present application, claim 63 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including an analog integrated circuit (IC) adapted for use in a transmit signal path of a communication device, and responsive to an input differential current signal generated externally as a function of a reference signal and a digital data input, the analog IC being coupled to a reference circuit for generating the reference signal, and comprising a circuit element for generating an output signal on the basis of the differential current signal.

Regarding claim 23 of the present application, claim 64 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the reference signal is a voltage reference signal.

Regarding claim 24 of the present application, claim 65 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the voltage reference signal is generated on the basis of a bandgap reference voltage.

Regarding claim 25 of the present application, claim 66 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the reference signal is a current generated from a reference voltage and a resistor.

Regarding claim 26 of the present application, claim 67 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the output signal is a voltage signal and the resistor is external to the analog integrated circuit.

Regarding claim 27 of the present application, claim 68 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the output signal is a current signal and the resistor is implemented on the analog integrated circuit.

Regarding claim 28 of the present application, claim 69 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.

Regarding claim 29 of the present application, claim 70 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the circuit element is a modulator.

Regarding claim 30 of the present application, claim 71 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.

Regarding claim 31 of the present application, claim 72 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein each current source in the modulator provides a bias current that is related to the reference signal.

Regarding claim 32 of the present application, claim 73 of U.S. Patent No. 6,615,027 encompasses all the claimed limitation including wherein the modulator performs direct up conversion.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Quochien B. Vuong
June 26, 2006.